Remarks

Claims 1 - 24 are presently active.

In the office action dated 11 October 2002 ("Office Action"), the drawings were objected to; claims 11 and 13 were objected to; claims 1, 8-11, 13, 15, 18, and 21-24 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicants' admitted prior art (Fig. 1); and claims 2-7, 12, 14, 16, 17, 19, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' admitted prior art (Fig. 1).

The various objections and rejections raised in the Office Action are addressed below.

Objections to the drawings

A set of corrected formals (Fig. 2 is corrected) are submitted under a separate letter.

Objection to claims 11 and 13 because of an informality

Claims 11 and 13 are amended to correct an informality.

35 U.S.C. §102(a) rejection of claims 1, 8-11, 13, 15, 18, and 21-24 over Applicants' Fig. 1

Applicants respectively traverse the rejection of claims 1, 8-11, 13, 15, 18, and 21-24.

Regarding the rejection of claims 1 and 15, it is argued on page 3 of the Office Action that the statement "a NAND gate (112,114) having a first input port (gate of 112) connected to the node (via 106) and an output port..." is found in Applicants' Fig. 1. This may be the case if transistors 112 and 114 of Applicants' Fig. 1 are identified as a NAND gate. However, this is not what claim 1 recites. Claim 1 recites "a NAND gate having a first input port connected to the node and an output port..." (underlining added). Note that "via an inverter (106)" or some such similar language modifying the term "connected" is not recited in claim 1.

The term "connected" is a term of art. Someone of ordinary skill in the art (circuit design) would interpret the phrase "A connected to B" to mean that A is directly

connected to B. That is, A is connected to B via an interconnect, such as metal or some other low resistance conductor. It does not mean that A is connected to B via a device (e.g., transistor, logic gate) or other passive circuit element (e.g., inductor, resistor, or capacitor). In contrast, it is recognized that the term of art "A is coupled to B" may mean that A is connected to B via a device or circuit element. Therefore, Applicants believe that claim 1, and claim 15 by virtue of its dependency upon claim 1, are not anticipated by Applicants' Fig. 1.

Regarding the rejection of claims 8-11, 13, 21-23, claim 8 recites in the last "wherein" clause that "the first transistor and the logic gate provide a keeper function to the node if and only if the second input port of the logic gate is at a voltage indicative of the dynamic circuit being in the burn-in condition." The argument in the Office Action, page 3, identifies the "first transistor" of claim 8 with transistor 108 of Applicants' Fig. 1. However, making such an identification does not satisfy the above quoted recitation of claim 8. The transistor 108 provides a keeper function to the node without the dynamic circuit being in the burn-in condition. Note that the drain of transistor 108 is connected node 110 and its gate is connected to inverter 106. During an evaluation phase, it will keep node 110 HIGH if it is not pulled LOW by nMOS network 102. Thus, it will provide a keeper function whether or not the dynamic circuit is in the burn-in condition. Therefore, Applicants believe that claim 8, and claims 9, 10, 11, 13,and 21-23 by virtue of their dependency upon claim 8, are not anticipated by Applicants' Fig. 1.

Regarding the rejection of claim 18, note that claim 18 depends upon claim 5. No discussion of a 35 U.S.C. §102(a) rejection of claim 5 appears in the Office Action. Nevertheless, claim 5 recites "a first transistor responsive to the output port voltage of the NAND gate to pull the node HIGH only if the second input port of the NAND gate is HIGH." If the first transistor is identified with transistor 108 of Applicants' Fig. 1, and if the NAND gate is identified with transistors 112 and 114 of Applicants' Fig. 1, then note that it is not true that transistor 108 pulls the node HIGH only if the second input port of the NAND gate is HIGH. The statement "A only if B" is logically equivalent to the statement "if A, then B." But clearly if transistor 108 pulls node HIGH, it does not follow that the second input port of the NAND gate must be HIGH. Therefore claim 5, and

claim 18 by virtue of its dependency upon claim 5, are not anticipated by Applicants' Fig. 1.

The argument regarding claim 24 is identical to the argument regarding claim 1 above.

35 U.S.C. §103(a) rejection of claims 2-7, 12, 14, 16, 17, 19, and 20 over Applicants' Fig. 1.

For the 35 U.S.C. §102(a) rejection of claims 1, 8-11, 13, 15, 18, and 21-24, all of the independent claims were discussed. Therefore, the above discussion also applies to claims 2-7, 12, 14, 16, 17, 19, and 20, and consequently Applicants do not believe that Applicants' Fig. 1 renders these claims obvious.

Respectfully submitted,

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